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LOW-POWER AND AREA-EFFICIENT MODIFIED CARRY SELECT ADDER (MCSA) WITH SINGLE RCA & BEC

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Abstract— The increase in the popularity of portable systems as well as the rapid growth of the power density in integrated circuits have made power dissipation one of the important design objectives. Adders are one of the most widely used components in integrated circuits(ICs), designing such efficient adders has been the goal in Very Large Scale Integrated (VLSI) design. Design of area and power efficient high speed data path logic systems are one of the most substantial areas of research in VLSI system design. In every digital adder, time required for the propagation of a carry through the adder decides the speed of the addition operation. The sum for each bit position in an adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The Carry Select Adder (CSA) is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the Carry Select Adder is not area efficient because it uses multiple pairs of ripple carry adders to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the multiplexers. The basic idea of this paper is to use binary to excess converter instead of Ripple Carry Adder (RCA) with in the regular CSA to achieve lower area and power consumption. The main advantage of this Binary to Excess Converter (BEC) logic comes from the lesser number of logic gates than the bit full adder structure.

Keywords— Carry Select Adder (CSA); Ripple Carry Adder(RCA); Binary to Excess Converter(BEC); Very Large Scale Integrated designs.

I. INTRODUCTION

Addition usually impacts widely the overall performance of digital systems and a all the arithmetic functions. Generally in every electronic application adders are most widely used. Multipliers, Digital Signal Processing (DSP) use this application to execute various algorithms.

Adders come in to the picture whenever multiplication operation is adopted. Millions of instructions per second are performed in microprocessors. So the speed of operation is the most important constraint to be considered while designing multipliers. Due to device portability, device should be designed for high performance and power consumption should be low. various devices like mobile, laptops and other lectronic devices requires more battery backups. An adder or summer is a digital circuit that performs addition of numbers. In modern computers adders reside in the arithmetic logic unit where other operations are performed [1][2][3].

Power dissipation is one of the most important parameter considered in all integrated circuits same as speed. Designing a efficient adder is of much concern for researchers same as that of the adders used as components in many circuits.

The comparison is done on the basis of three performance parameters i.e. area, speed and power consumption. This paper presents a modified carry select adder designed in various stages. The Results obtained from modified carry select adders are best in area and power consumption. The CSA is used in many computational systems to make the problem of carry propagation delay easier by independently generating the multiple carries and select a carry to generate the sum. However, the Carry Select Adder is not area efficient because it uses multiple pairs of Ripple Carry Adder to generate partial sum and carry by considering carry input as zero and one, then the final sum and carry are selected by the Multiplexers [4][5].

II. EXISTING SYSTEM

In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry are the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output.

Fig.1 shows the block diagram of conventional 16bit CSA. It has five groups of different size RCA.

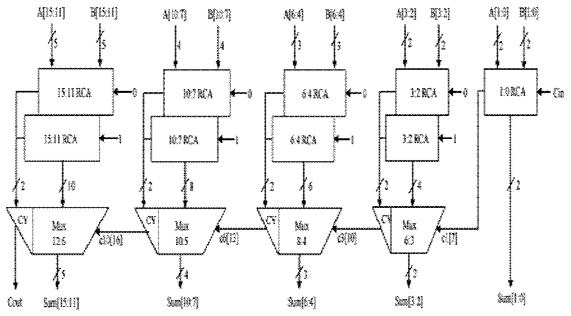

Fig 1 : Block diagram of 16 Bit CSA

The layout of a ripple carry adder shown in fig 2 is simple, which allows for fast design time, however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder.

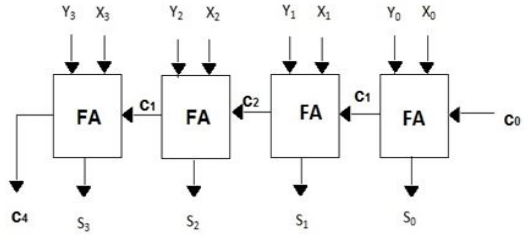

Fig 1 : Ripple Carry Adder Circuit Diagram

The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic.

III. PROPOSED SYSTEM

A Modified Carry Select Adder (MCSA) design is proposed, which make use of single RCA and BEC instead of using dual RCAs to reduce area and power consumption with small speed penalty. As the base of proposed design is that the number of logic gates used in BEC is less than that of ripple carry adder.

Thus BEC replaces the ripple carry adder with Cin=1 instead of using dual RCAs to reduce area and power consumption of the conventional carry select adder. To replace the n-bit RCA, an n+1 bit BEC is required. The importance of binary to excess converter logic comes from the large silicon area reduction when designing MCSA for large number of bits.

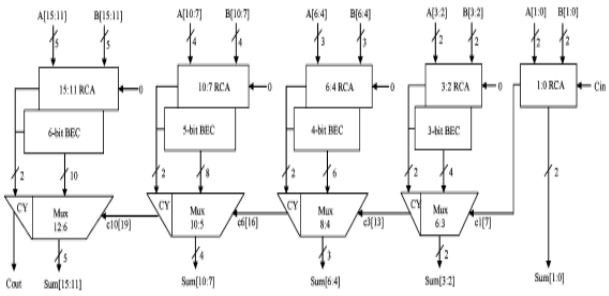

Fig 3 : Modified 16 Bit CSA

Fig 3 shows the structure of the proposed 16-b SQRT CSLA using BEC for RCA with C_{in}=1 to optimize the area and power [6][7].

IV. SIMULATION RESULTS BY XILINX ISE

Fig. 4 the simulation results are obtained from Modelsim, Xilinx and cadence. The cadence analog lab tool software provides virtuoso commands for the simulation of waveform.

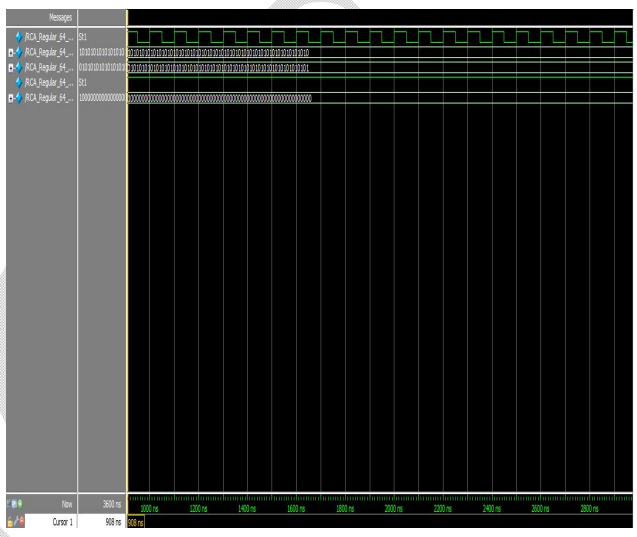

Fig 4 : Output Waveform of CSA using Modelsim

The output waveform of 64 bit carry select adder using binary to excess converter is shown in the fig 4. we could see that the given input data is 64 bit and the output data obtained is 64 bit with the carry output.

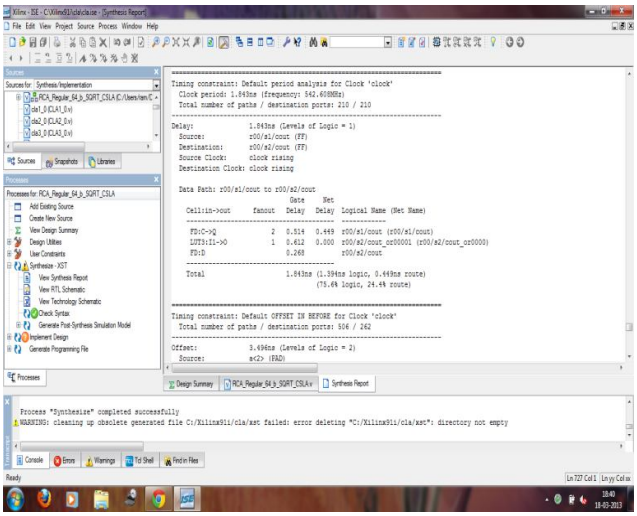

Fig 5 : Delay Output using Xilinx

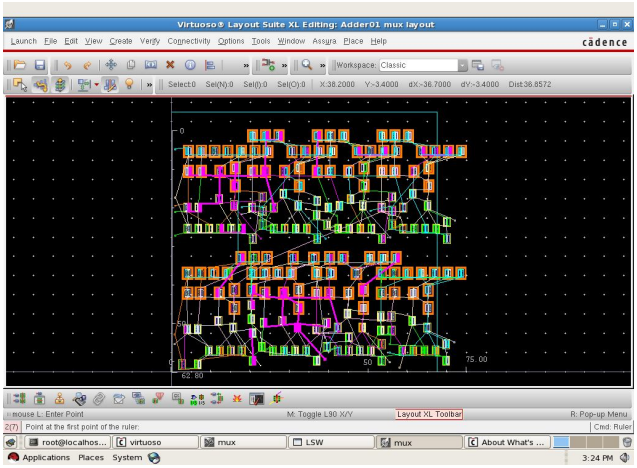

Fig 6 : Layout using Cadence-Virtuoso

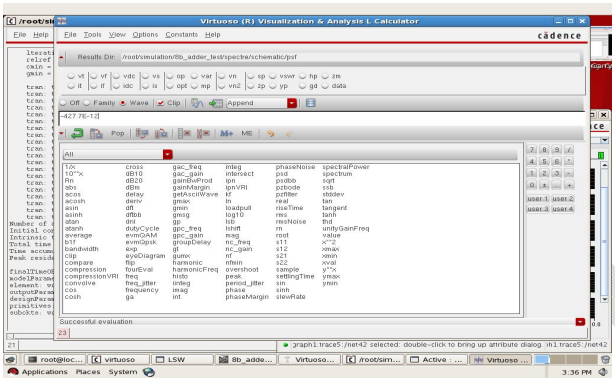

Fig 7 : Delay Output using Cadence-Virtuoso

V. PERFORMANCE ANALYSIS

We proposed a new adder design concept called carry select adder for low power and for area reduction. The operations of adder are differentiated according to their logic.

With the slight modification CSA adder design can be used in a 128 bit CSA stages for further reduction of area. While providing better energy efficiency throughout the proposed CSA adder design incurs minimal area and performance penalties.

TABLE I Comparison of CSA using Xilinx

Adder	Existing CSA	Proposed CSA
Delay	9.159ns	2.129ns
Area	9916	180
Power	2425mw	81mw

TABLE III Comparison of CSA using CADENCE tool

Logic	Binary	Pass transistor
Delay	170.8E-12	-427.7E-12
Area	6213µm^2	4710 µm^2
Power	12.85mw	16.81mw

VI. CONCLUSION

Thus the designed carry select adder using gate level modification had given various changes in the delay, power consumption. The delay and power consumption for carry select adder designed using RCA and multiplexer is 9.159ns and 2425mw .At the same time the delay and power consumption for carry select adder which uses BEC and mux has 2.129ns and 81mw.Thus the delay is reduced by 7.03ns and power consumption is also reduced by 2344mw.

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